

FIG. 1A

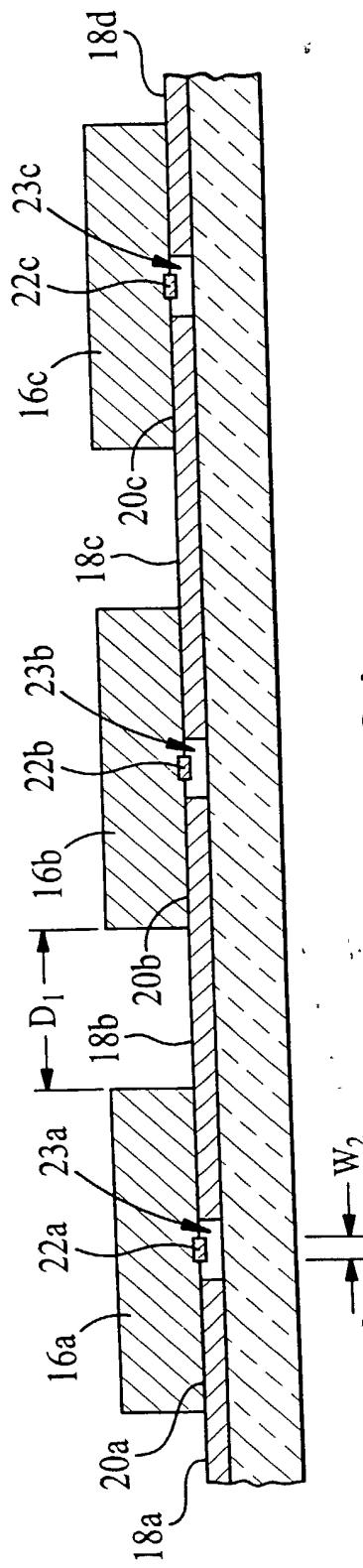
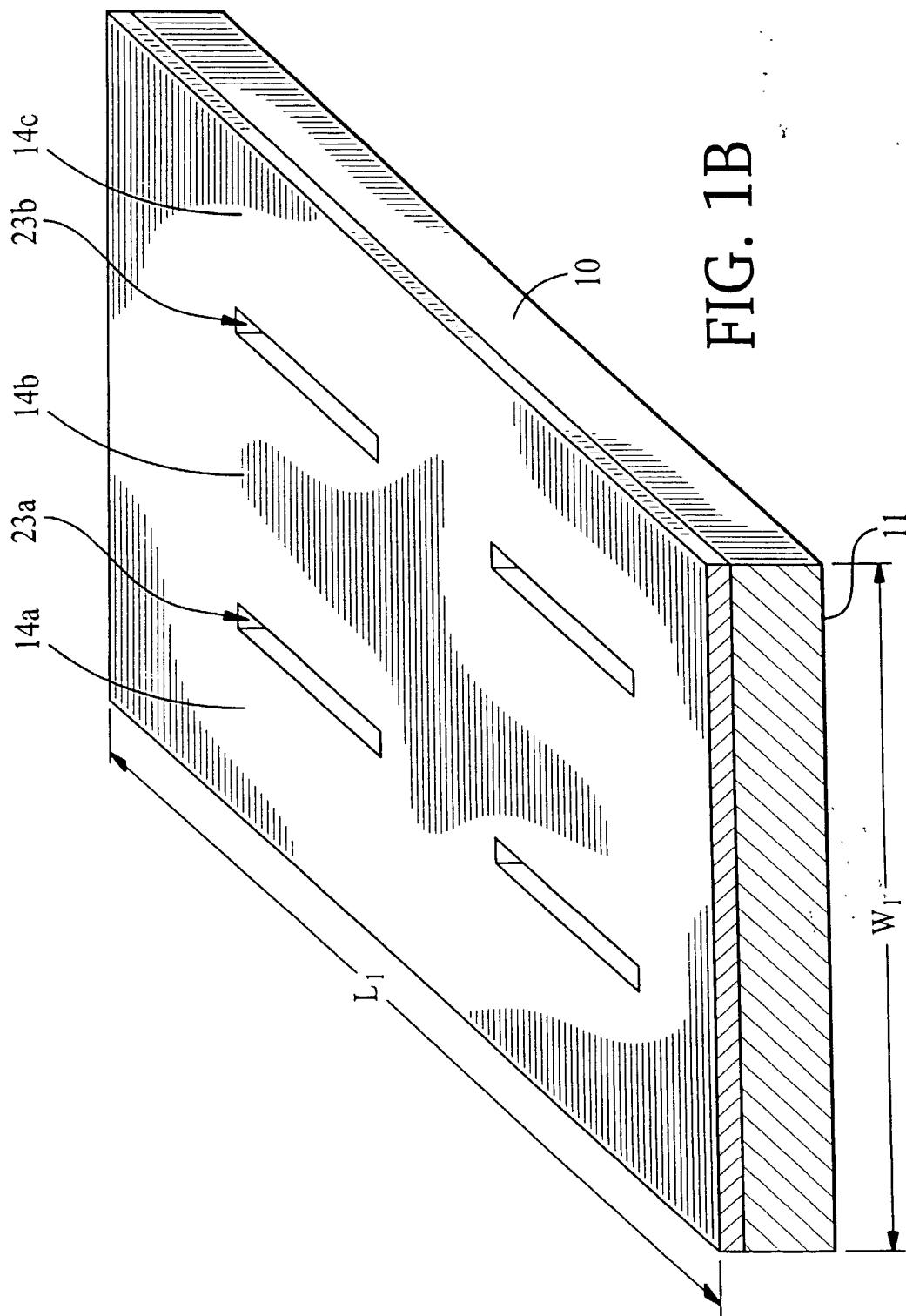


FIG. 2A



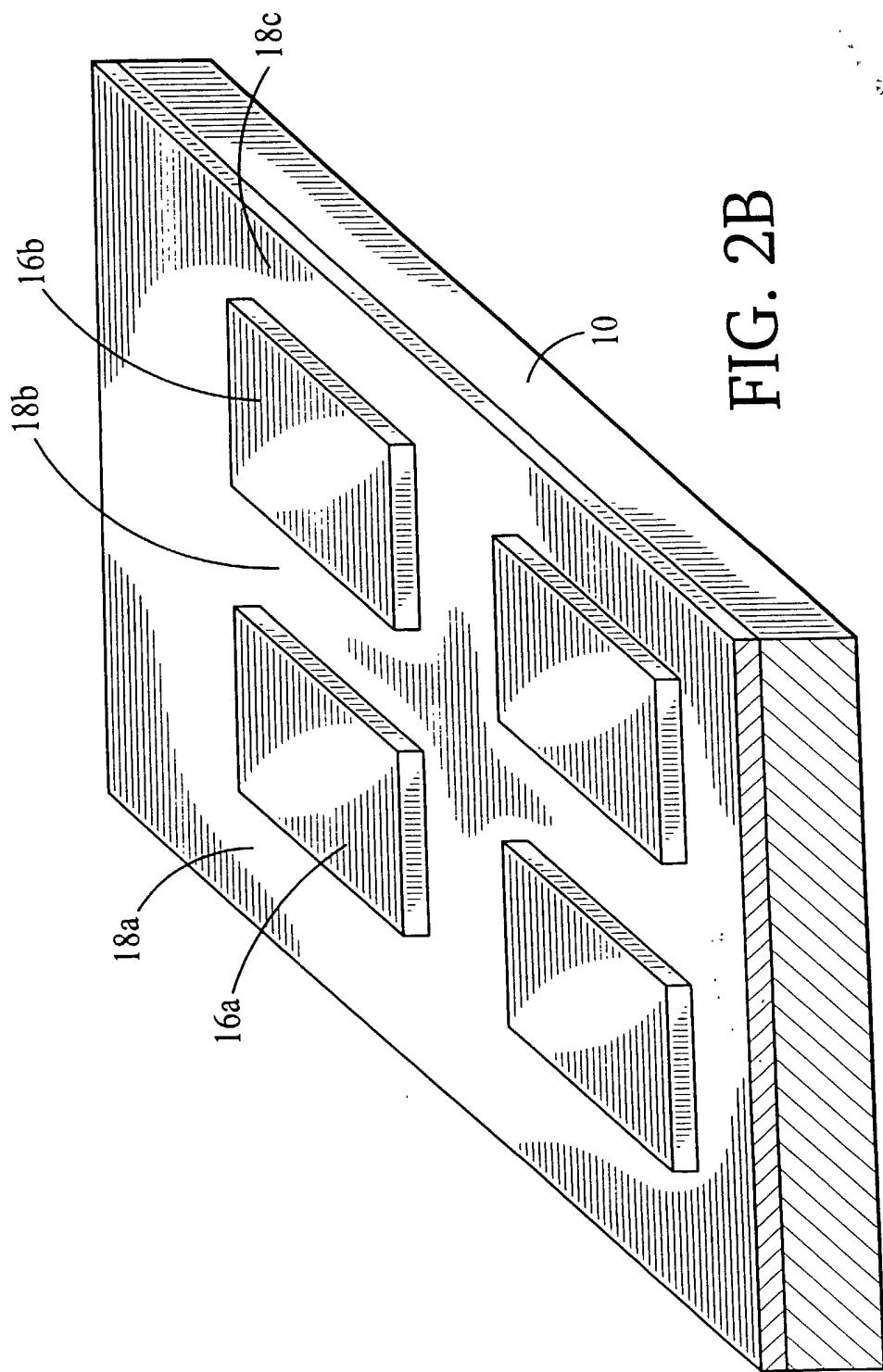


FIG. 2B

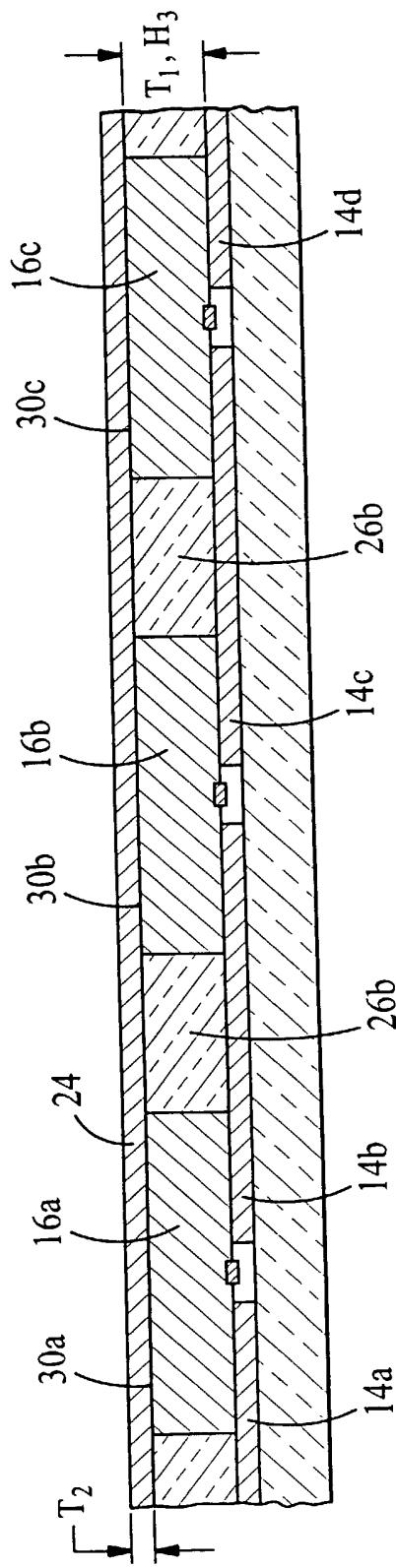


FIG. 3A

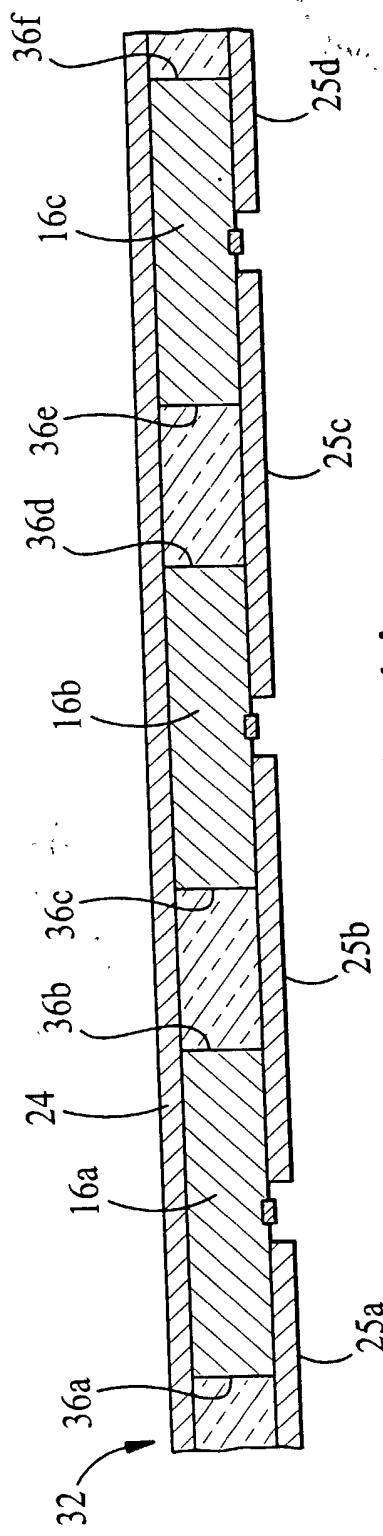


FIG. 4A

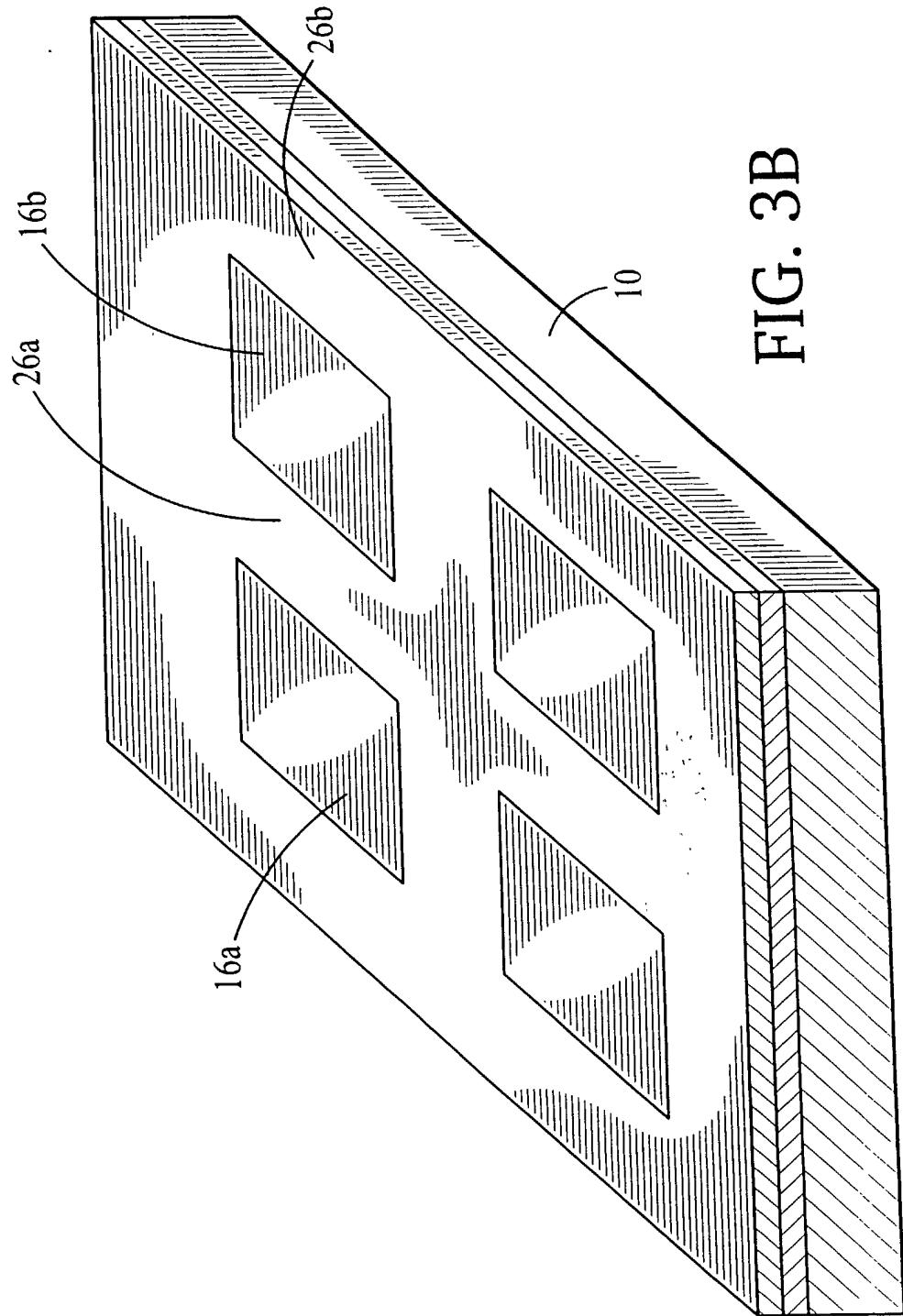


FIG. 3B

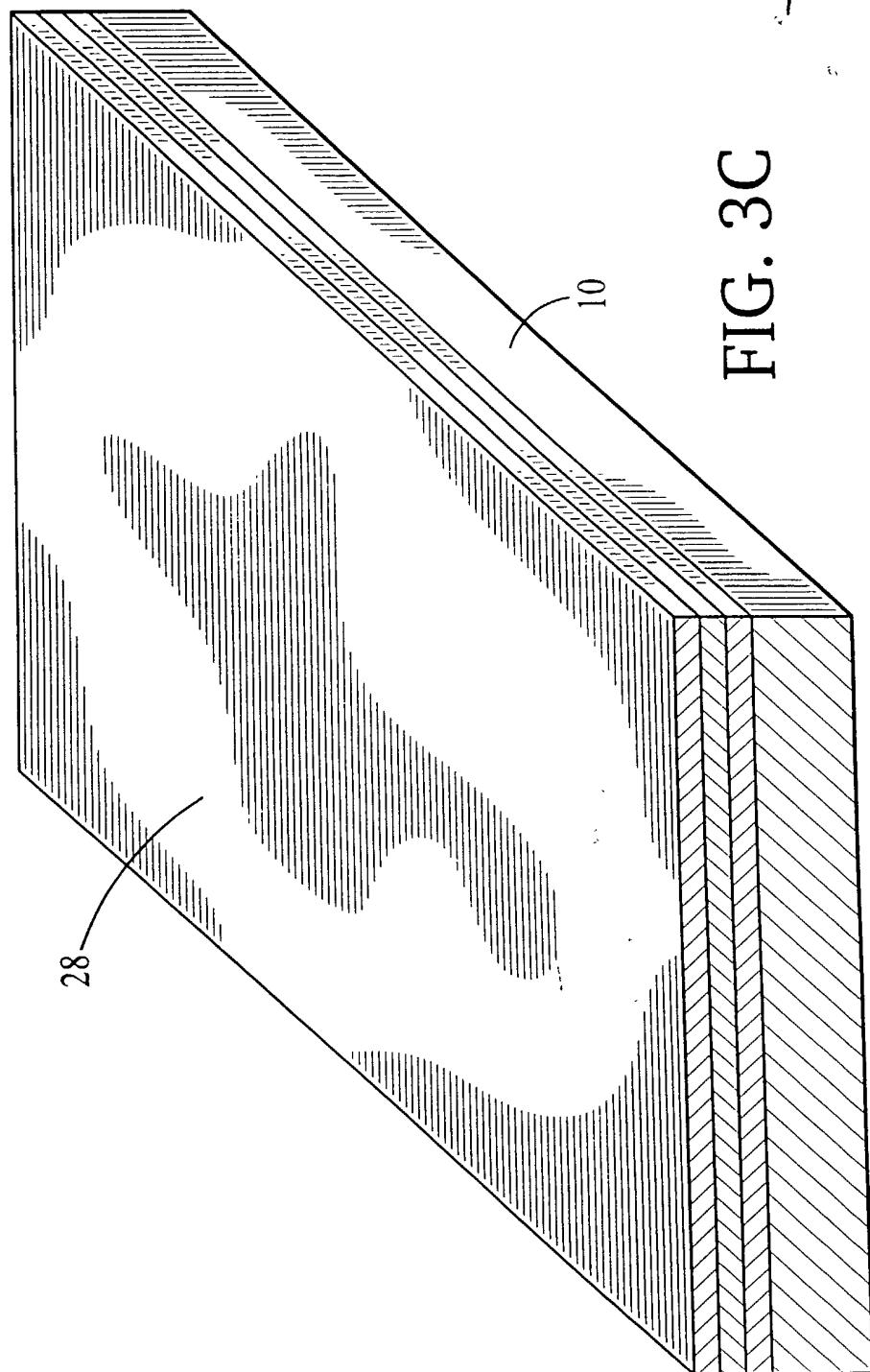


FIG. 3C

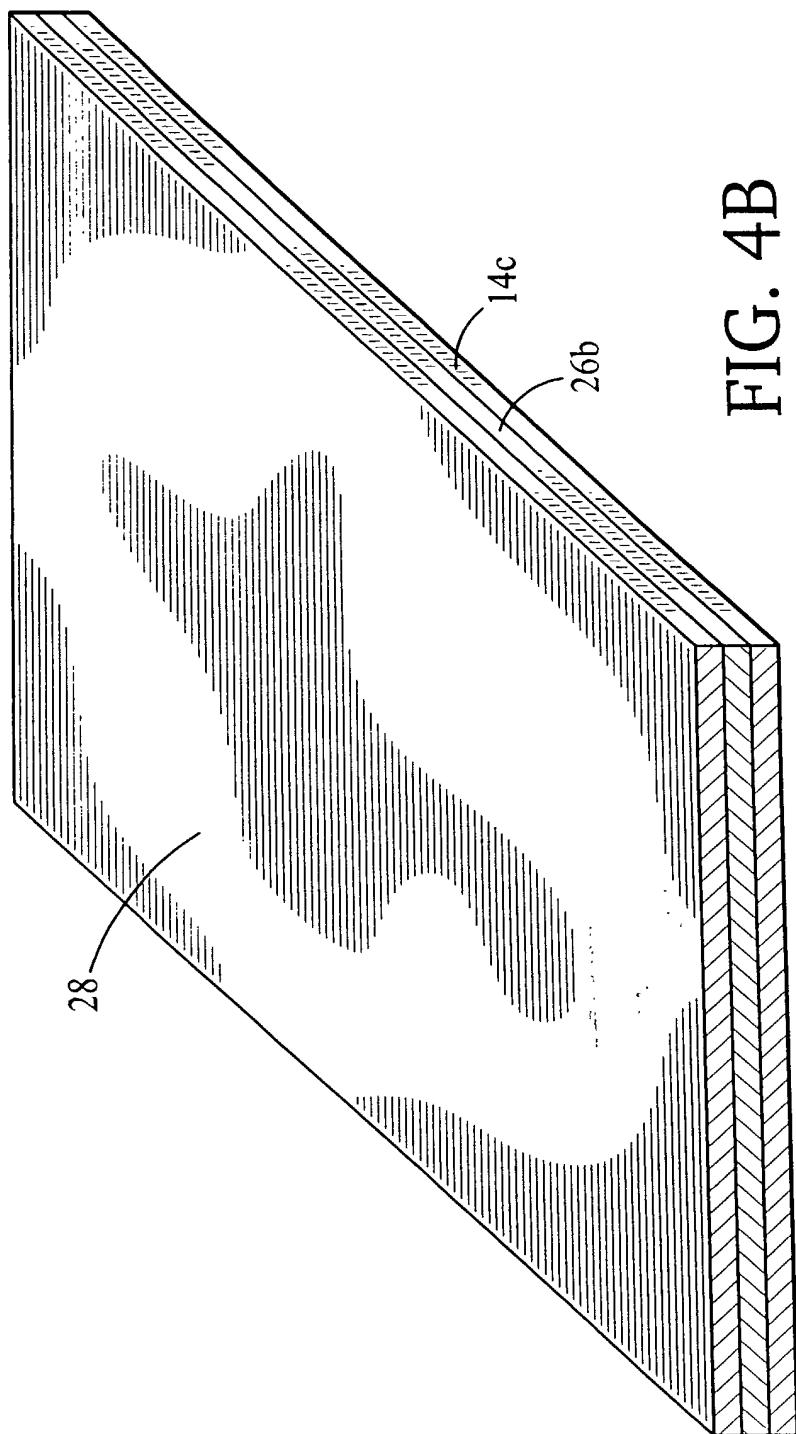


FIG. 4B

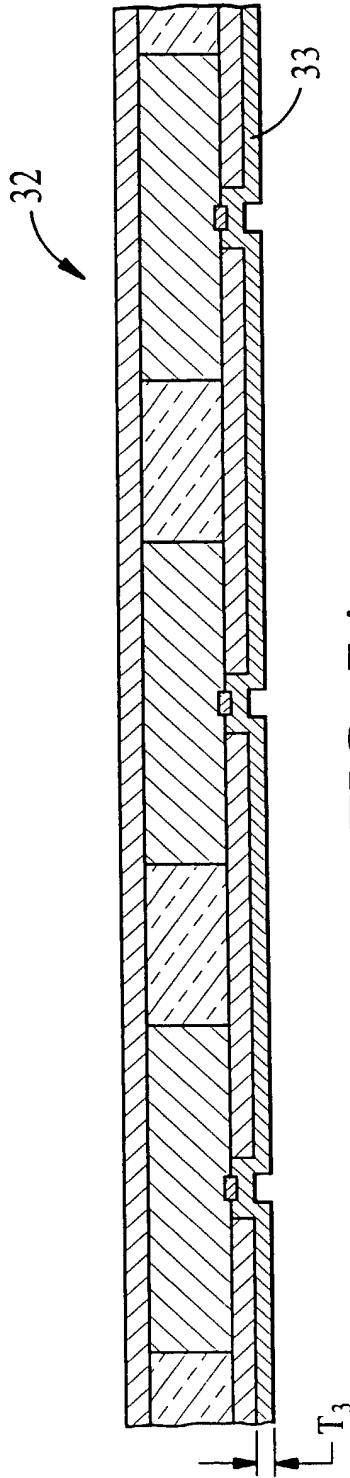


FIG. 5A

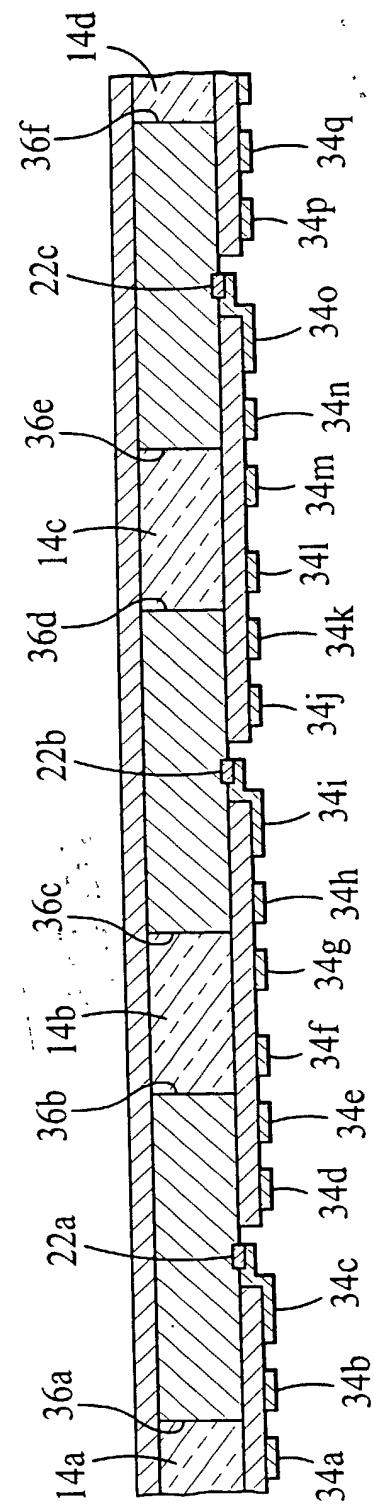


FIG. 5B

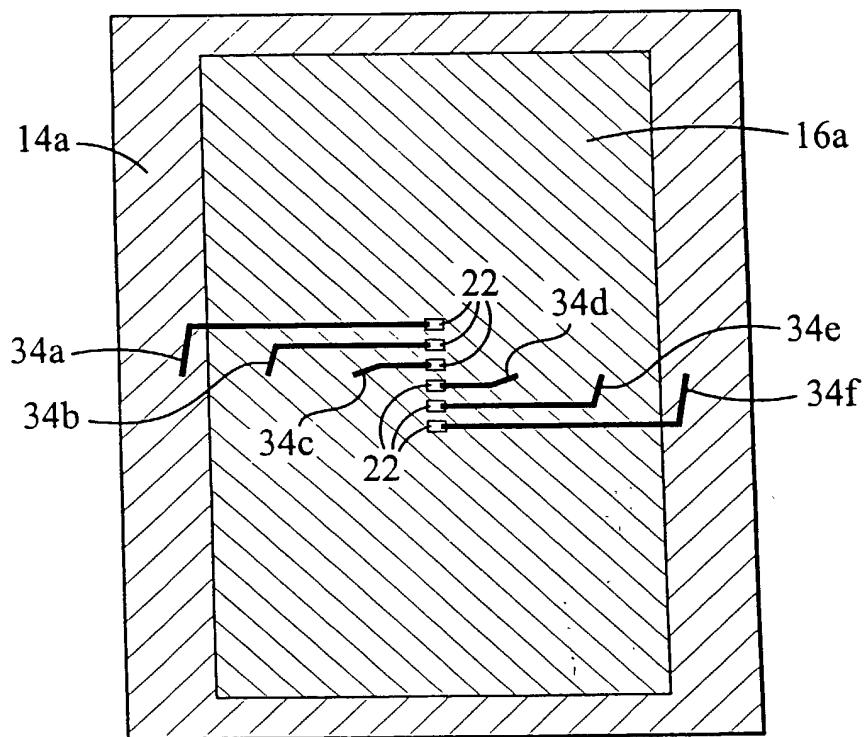


FIG. 5C

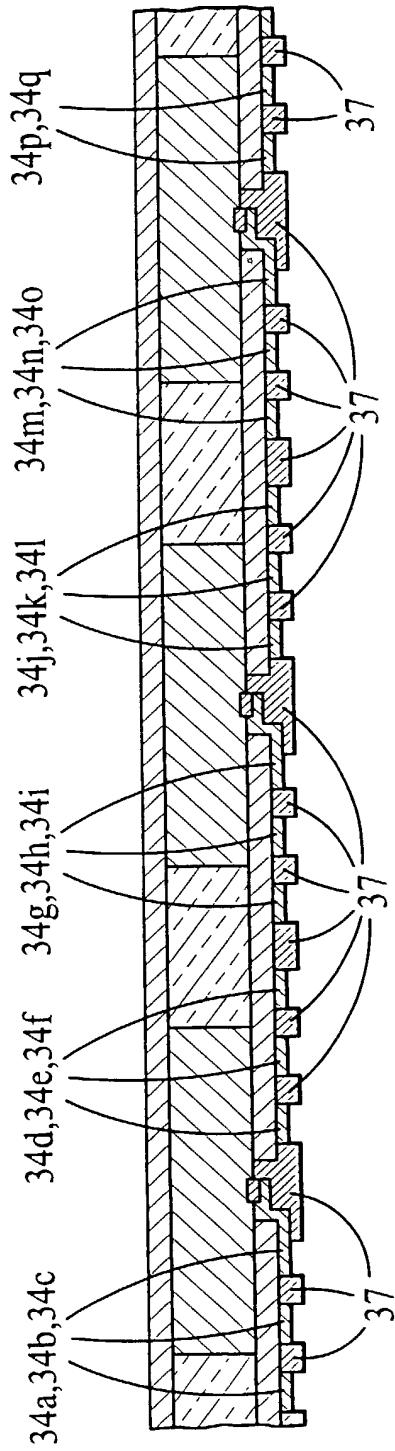


FIG. 5D

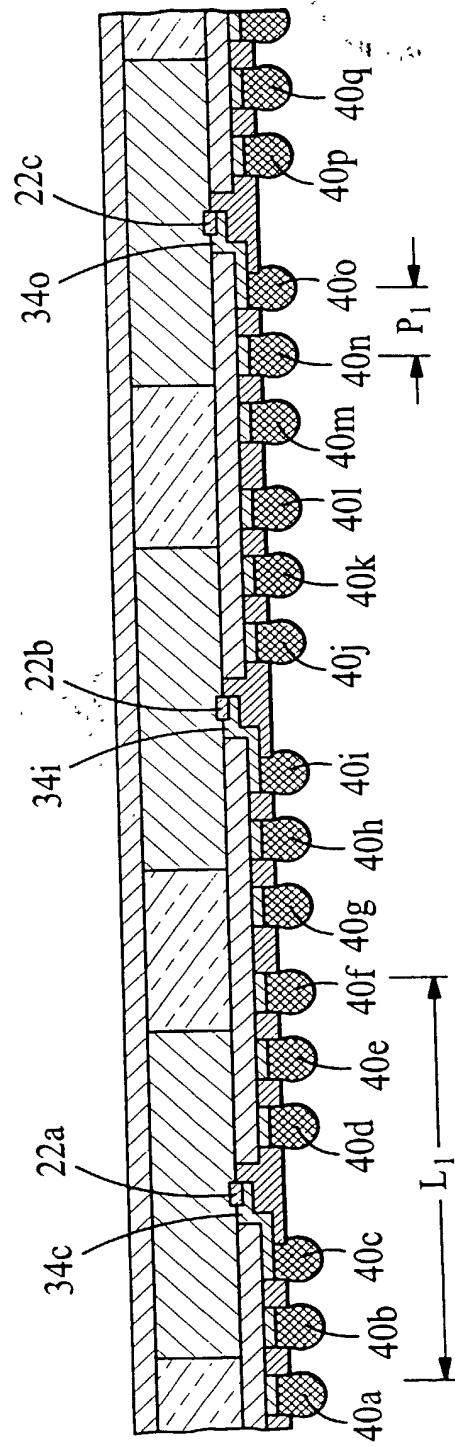


FIG. 6

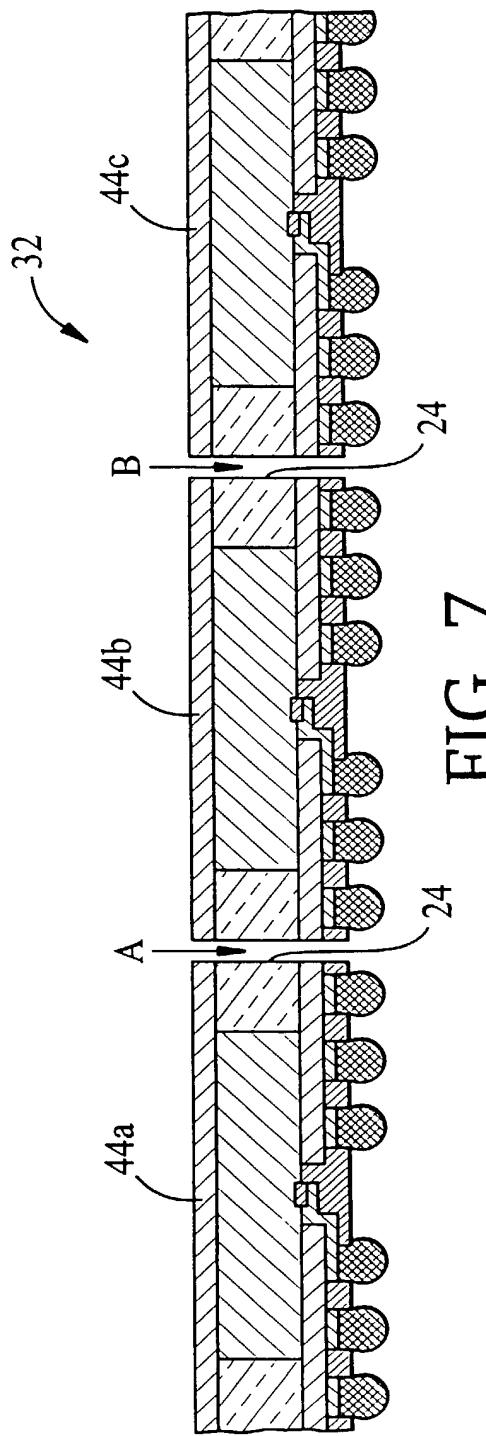


FIG. 7

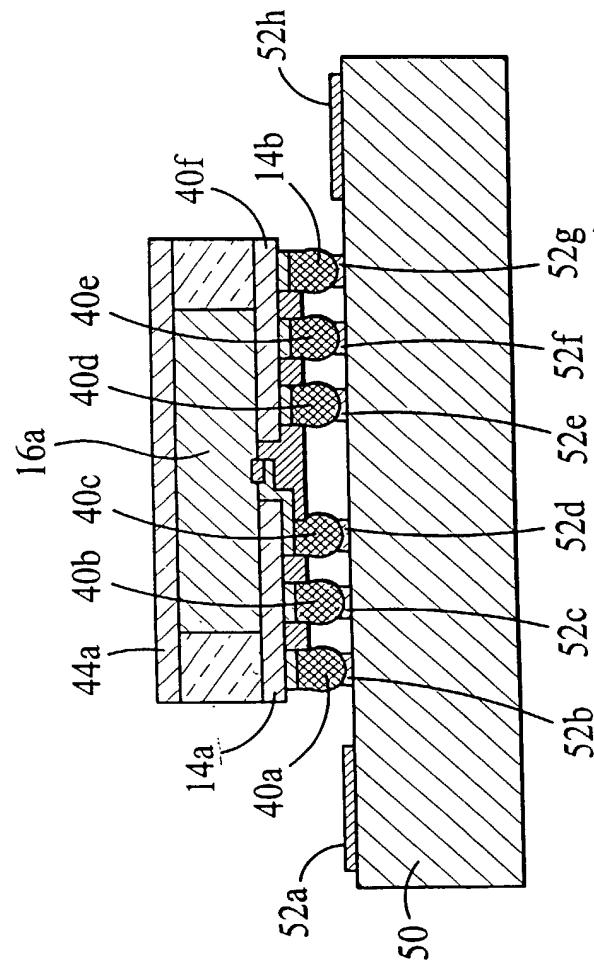


FIG. 8

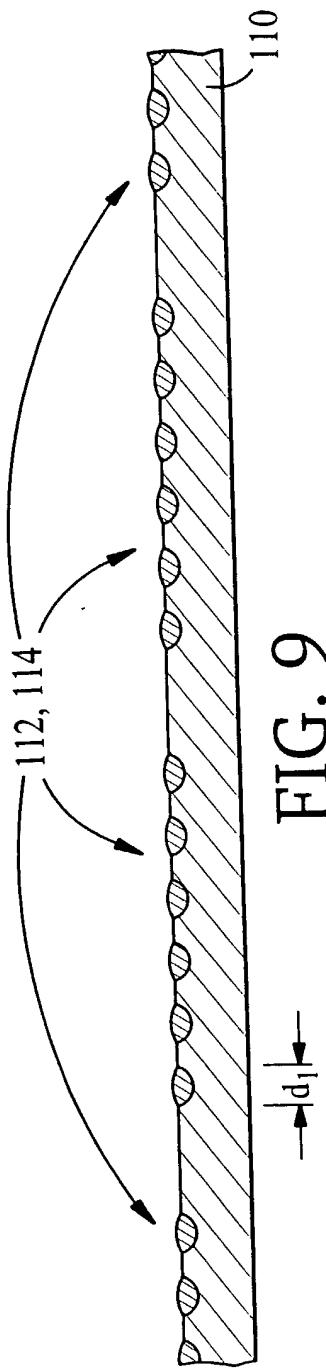


FIG. 9

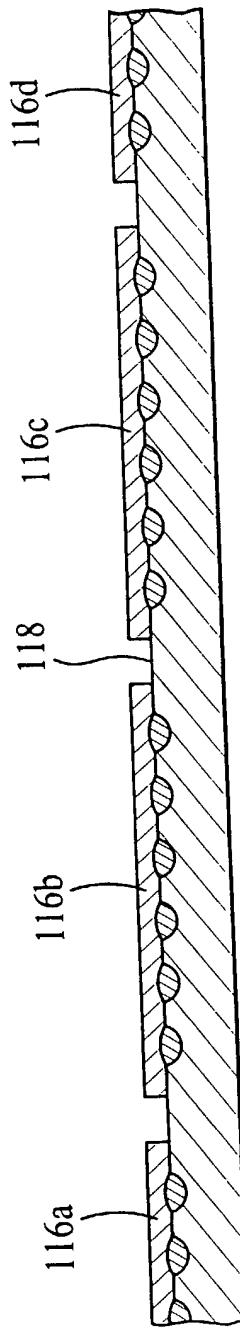


FIG. 10

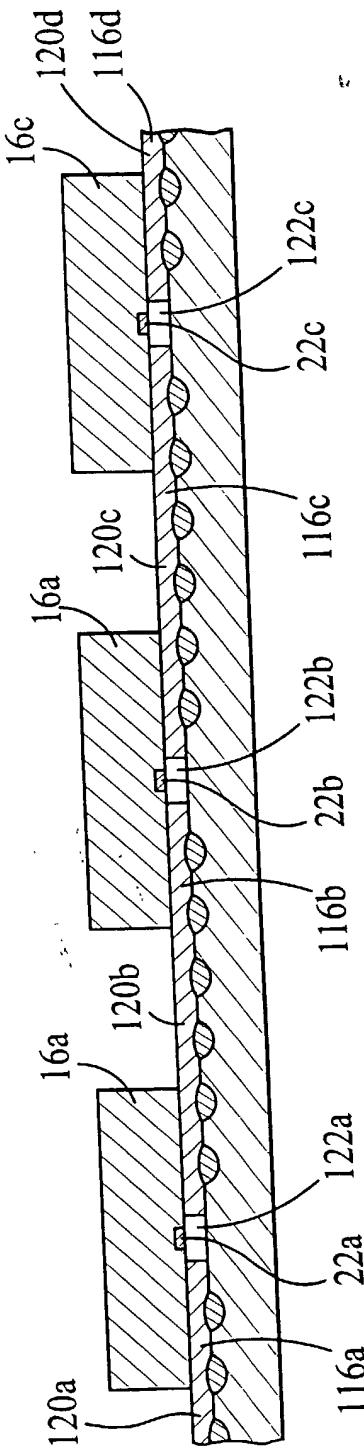
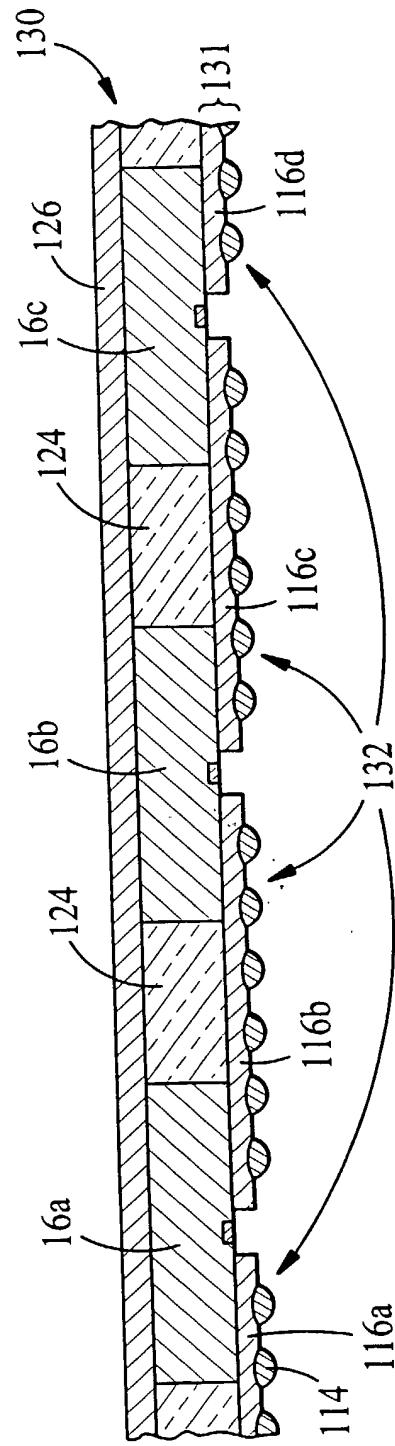
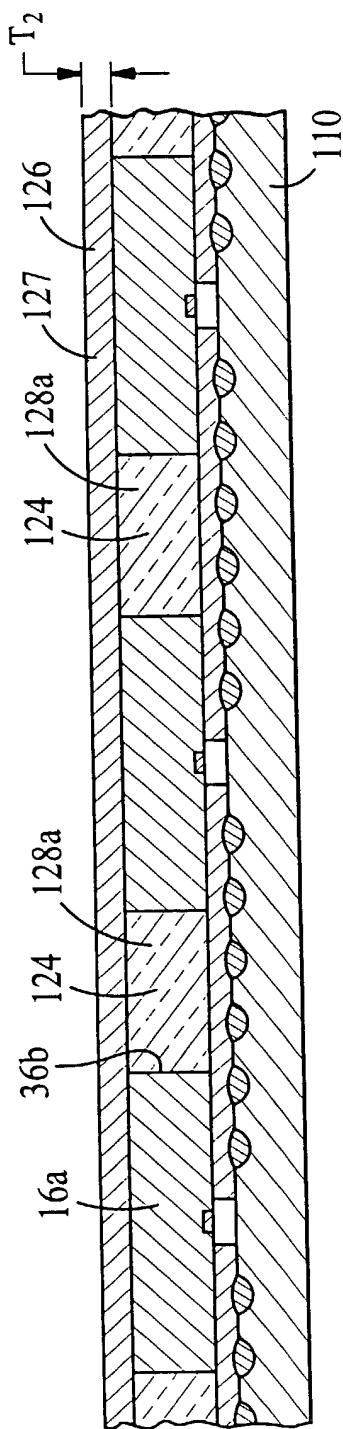


FIG. 11



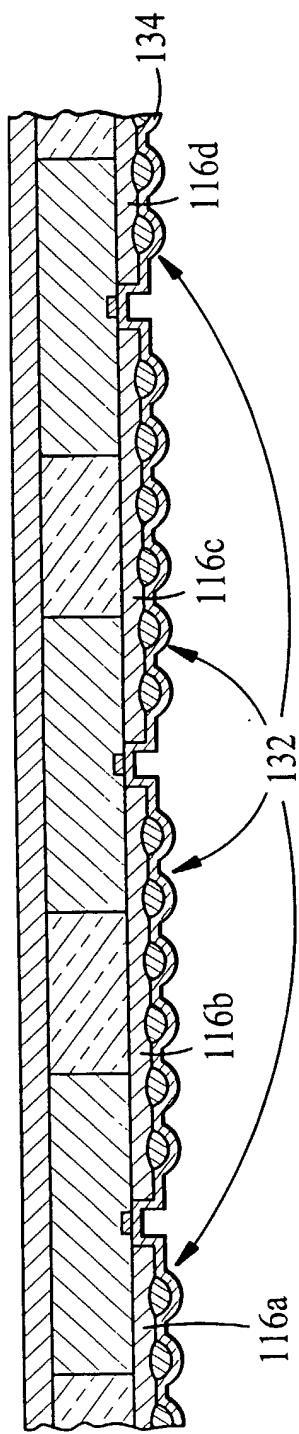


FIG. 14A

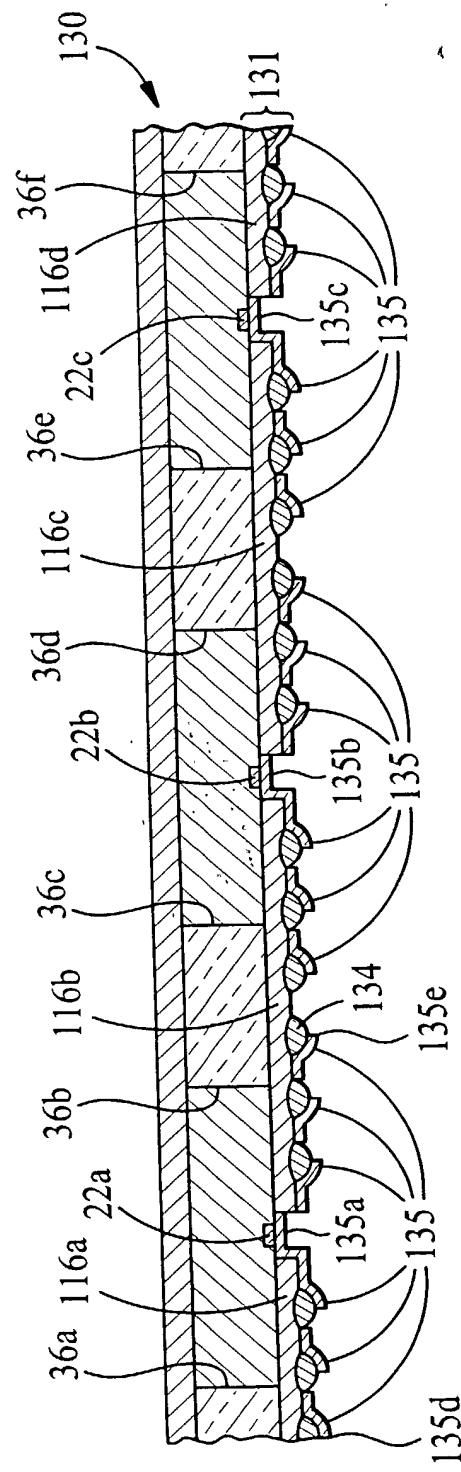


FIG. 14B

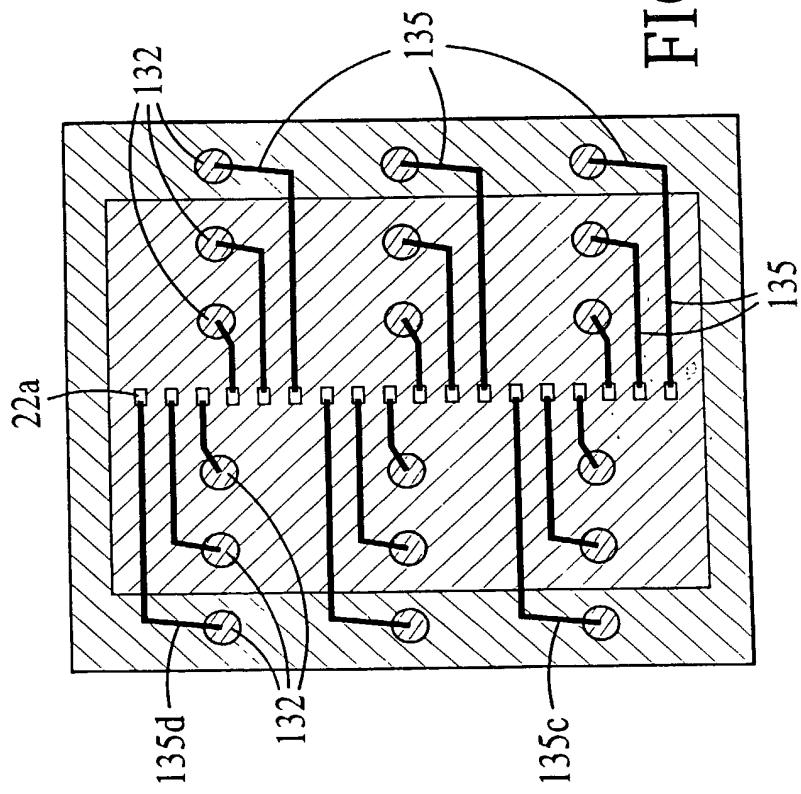


FIG. 14C

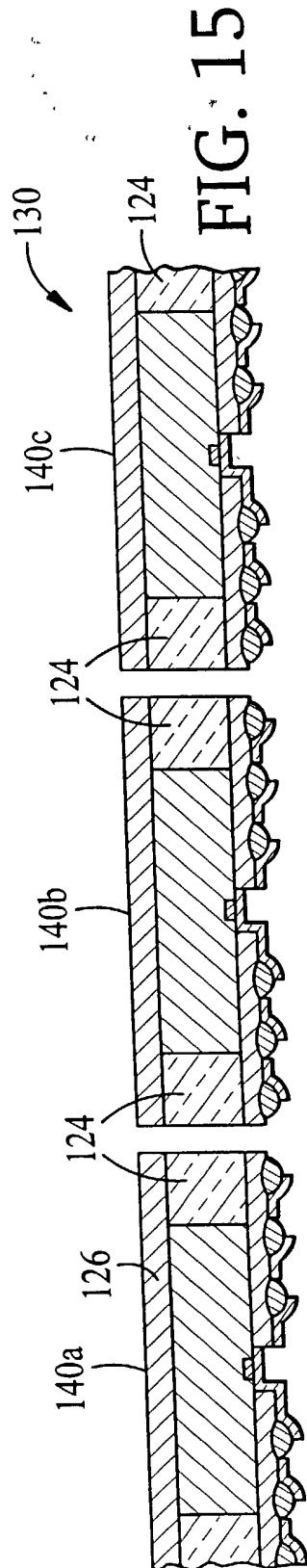


FIG. 15

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TRANSFER WAFER LEVEL PACKAGING

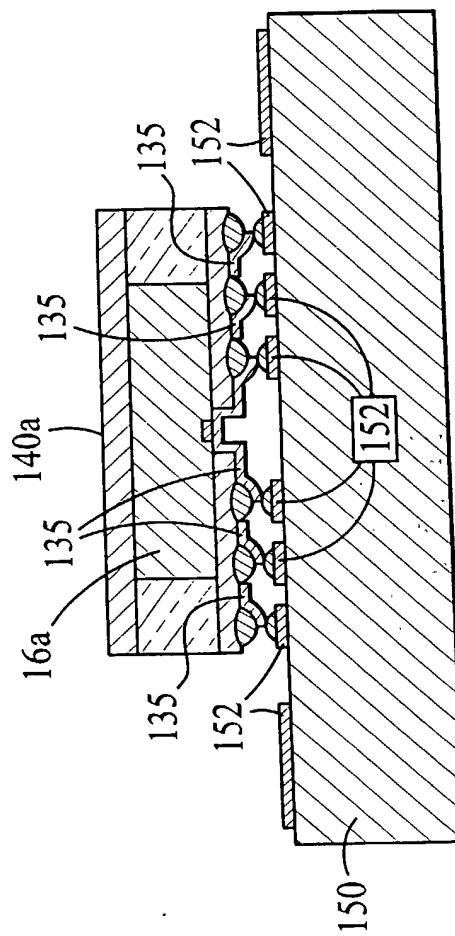
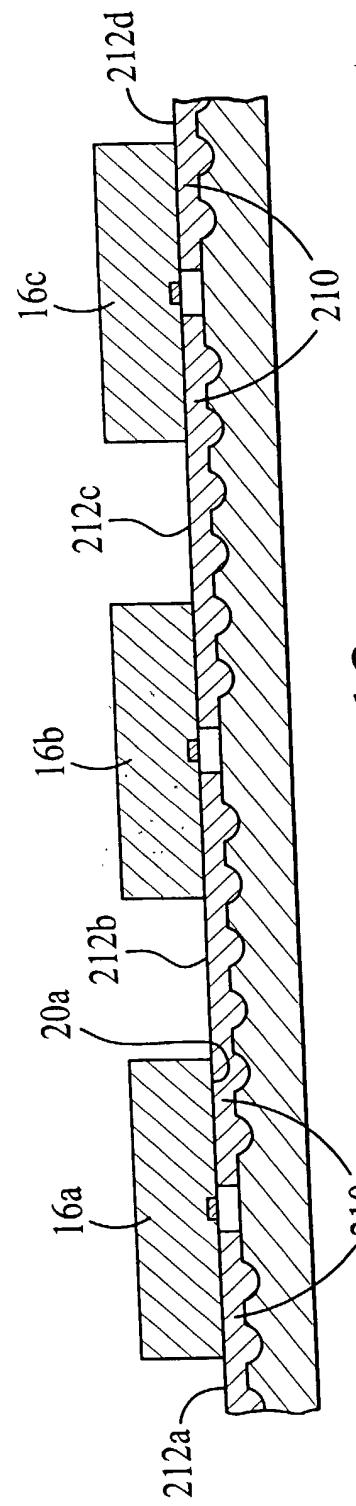
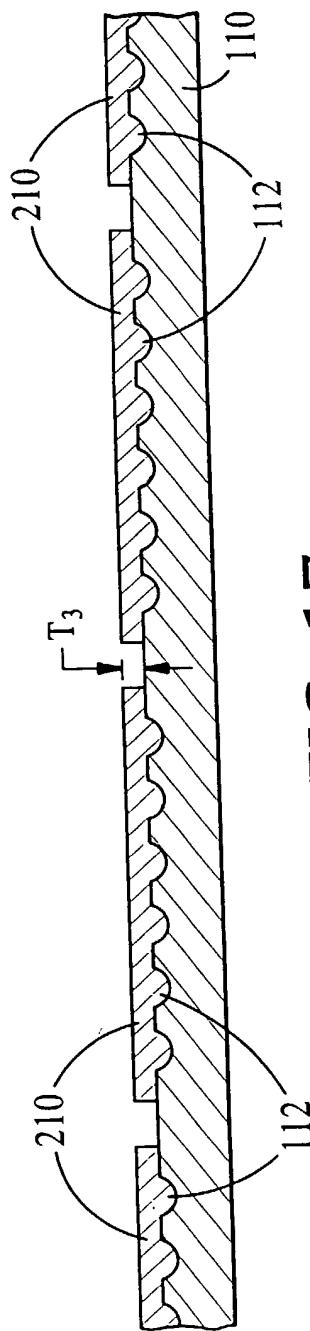


FIG. 16



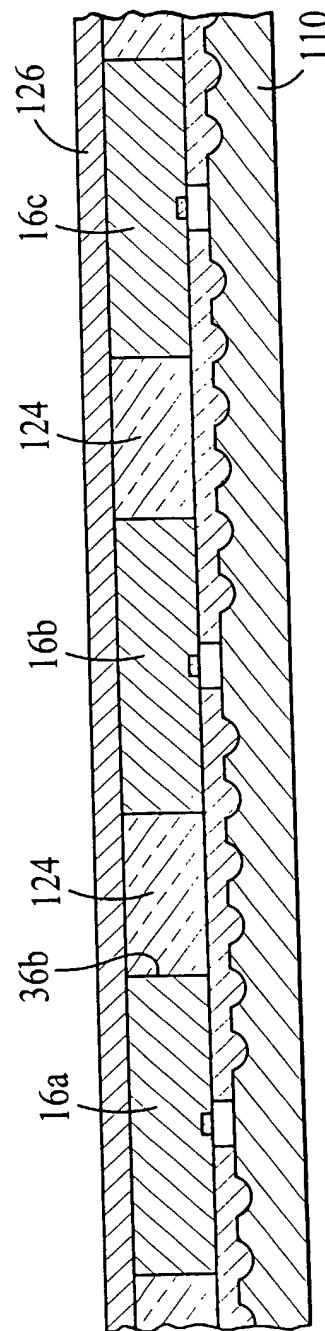


FIG. 19

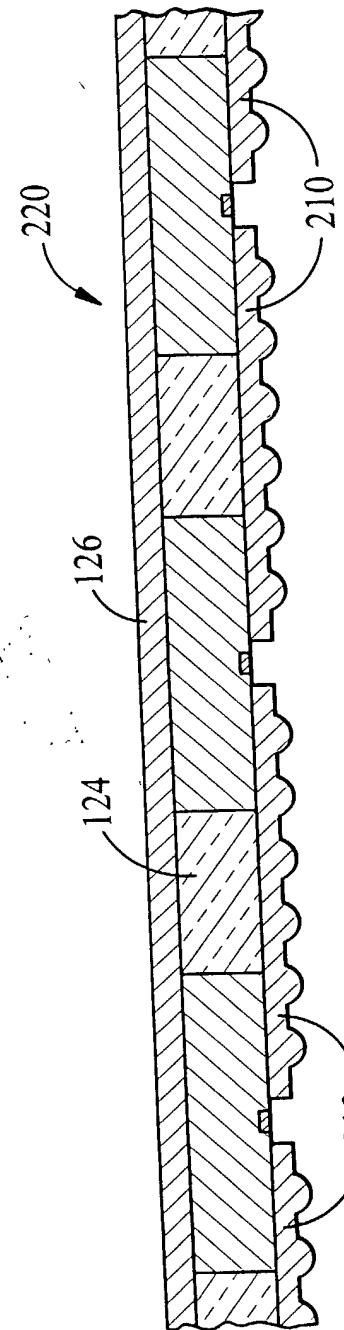


FIG. 20

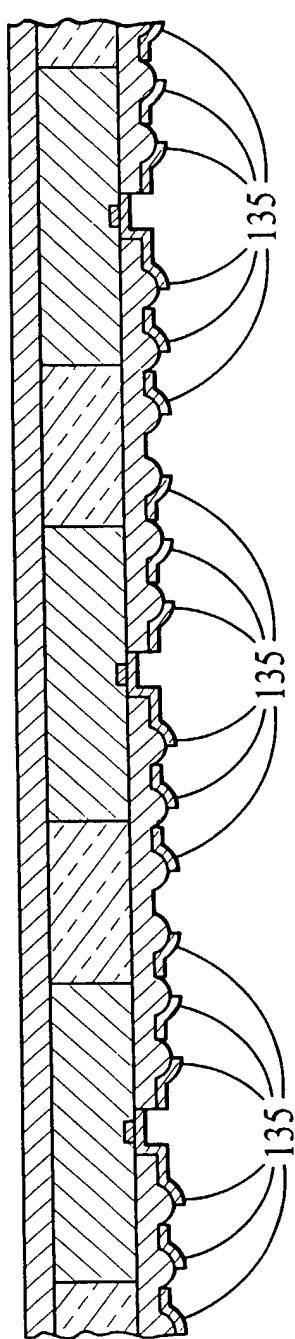


FIG. 21

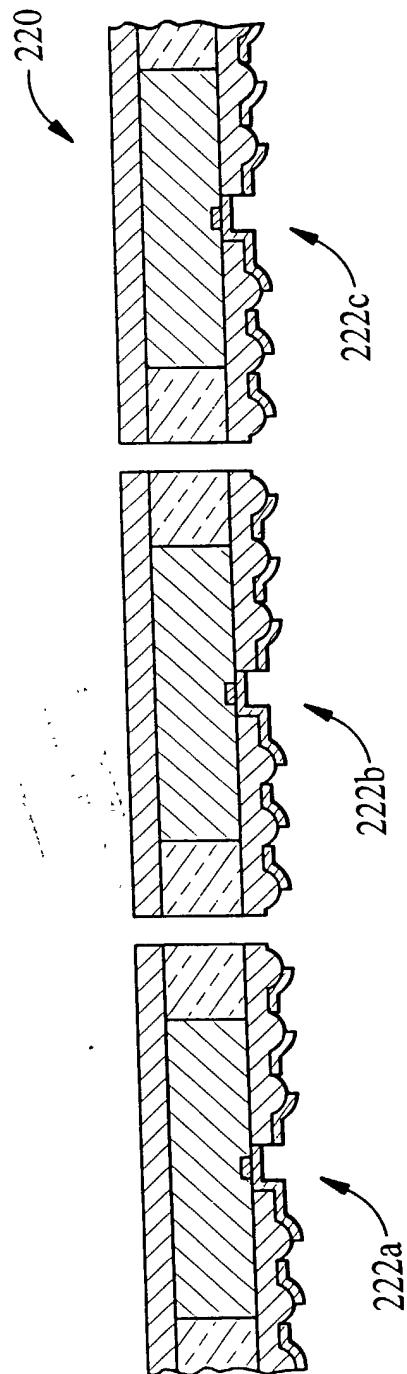


FIG. 22

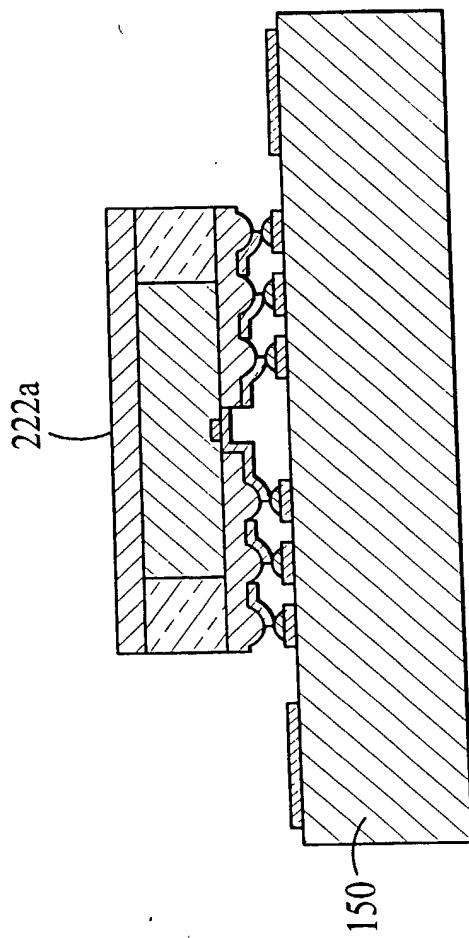


FIG. 23